

Digital Lock-In Detection for Discriminating Multiple Modulation Frequencies With High Accuracy and Computational Efficiency

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Abstract—We introduce a novel digital lock-in detection technique for simultaneously measuring the amplitude and phase of multiple amplitude-modulated signals. Using particular modulation and sampling constraints and averaging filters, we achieve optimal noise reduction and discrimination between sources of different modulation frequencies. Furthermore, it is shown that the digital lock-in technique can be performed as a simple matrix multiplication, which considerably reduces the computation time. The digital lock-in algorithm is described and analyzed under certain sampling and modulation conditions, and results are shown for both numerical and experimental data.

Index Terms—Digital lock-in detection, lock-in amplifier, optical tomography, phase-sensitive detection, spectroscopy, synchronous detection.

I. INTRODUCTION

IN GENERAL, lock-in detection is used to measure the amplitude and phase of narrow-band amplitude-modulated signals [1]. This detection technique requires reference signals that are modulated at the same frequencies as their signals of interest to use phase-sensitive detection. This enables a “locking in” to the frequency of interest while simultaneously ignoring all other frequencies. In this way, measuring very small ac signals that are buried in noise can be accomplished. The lock-in detection is utilized in the measurement systems for a wide range of applications that often suffer from low signal to noise.

Analog implementations have been the standard for lock-in detectors. However, increasing attention has been paid to digital techniques [2]–[9] because of the several advantages they hold over their analog counterparts. The main advantages are the rejection of unwanted dc signals and offsets, the better stability,

and the ability to measure lower frequency signals. Digital lock-in detection has already been used in instrumentation for a variety of applications including magnetometry [10], [11], optical spectroscopy [12], [13], and electrical impedance spectroscopy [14]. The later two applications often extend into tomographic imaging where it is desirable to measure signals from multiple sources in the frequency domain or from sources that have been frequency-encoded. Instrumentation for optical tomography [15], [16] and electrical impedance tomography [17] typically accomplishes this by simultaneously performing the lock-in detection at multiple modulation frequencies. Simultaneously detecting multiple signals at different modulation frequencies is complicated due to the fact that the different signals will interfere with each other. To the best of the authors’ knowledge, a digital lock-in technique has not specifically been designed and optimized for detecting multiple signals of different modulation frequencies.

In this paper, we introduce a digital lock-in detection technique with features that are ideal for simultaneously working with multiple modulation frequencies. This paper begins with the details of the digital lock-in detection for both the standard and multiple-frequency cases. Next, we show that if one uses an averaging filter and installs certain constraints on sampling and modulation frequencies, then the digital lock-in detection technique will have certain qualities that are ideal for discriminating between sources at different modulation frequencies. Finally, we will show an alternative way of formulating the digital lock-in technique that will allow for fast computation of the amplitude and phase.

II. DIGITAL LOCK-IN DETECTION

A. Standard Single-Frequency Lock-In Detection

Typically, in lock-in detection [1]–[9], there is a source signal

$$S(t) = dc_s + A_s \cos(2\pi f_m t + \varphi_s) \quad (1)$$

that is an input to some system that yields a measurable response $M(t)$, which is attenuated in the amplitude and shifted in the phase according to

$$M(t) = dc_m + A_m \cos(2\pi f_m t + \varphi_m). \quad (2)$$

The modulation frequency f_m is known. To gain some information about the system, one measures the amplitude A_m and the phase φ_m . Usually, the dc_m term is not a quantity of interest because it is highly contaminated with unwanted

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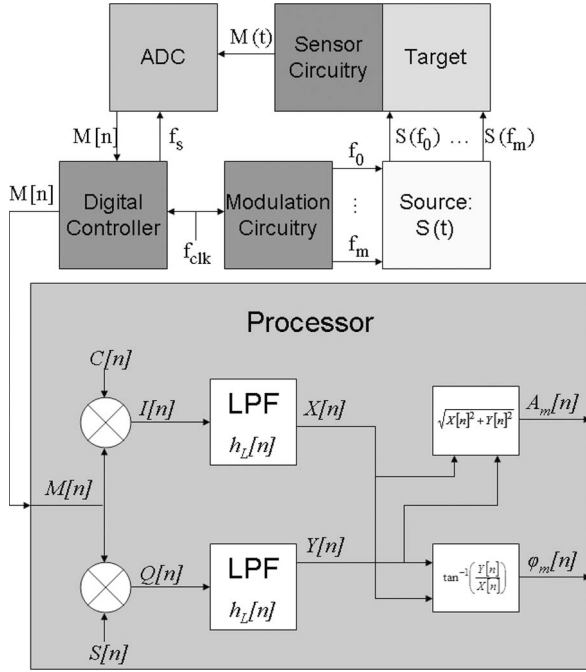


Fig. 1. Diagram of digital lock-in detection hardware and algorithm to be implemented in the digital domain.

environmental and/or systematic distortions. In analog lock-in detection, this $M(t)$ is multiplied with a reference signal of the same frequency by a mixer, and the result is passed through a low-pass filter. If the phase of the signal is unknown or a quantity of interest, quadrature detection is performed, which requires two reference signals that are a quadrature apart (cosine and sine). Fig. 1 shows a diagram for the basic hardware and computation algorithm used in digital lock-in detection [2]–[9]. The analog-to-digital converter (ADC) takes N_s samples of $M(t)$ at a sampling frequency f_s to yield the discrete signal

$$M[n] = \text{dc}_m + A_m \cos \left[\frac{2\pi f_m n}{f_s} + \varphi \right], \quad 0 \leq n \leq N_s - 1. \quad (3)$$

The time required to take N_s samples, which is referred to as the measurement time T_m , is

$$T_m = \frac{N_s}{f_s}. \quad (4)$$

Often, continuous monitoring of individual sources at rates as high as f_s is not necessary, and thus, the measurement time can also be viewed as the settling time of the lock-in filter. Since the noise reduction exhibited by the digital lock-in technique increases with T_m , N_s is chosen to compromise a tradeoff between high noise reduction and short measurement time T_m . The Nyquist criterion specifies that the sampling frequency must be greater than twice the sampled signal frequency

$$f_s > 2f_m. \quad (5)$$

After the data have been sampled, it is routed to a digital processing unit such as a personal computer (PC), a digital signal processor, or a field-programmable gate array (FPGA),

where the computational aspect of the digital lock-in detection is performed. Digital lock-in techniques require discrete signals

$$C[n] = \cos \left[\frac{2\pi f_m n}{f_s} \right] \quad (6)$$

$$S[n] = \sin \left[\frac{2\pi f_m n}{f_s} \right] \quad (7)$$

for the cosine and sine waves at the modulation frequency f_m .

These discrete signals for the cosine and sine can be obtained from a reference signal that is numerically generated and stored in the memory of the processing unit. Numerically generating these reference signals implies that they are free of any noise other than the numerical precision errors, but if the source modulation hardware and the sampling of the ADC are not synchronized, there might be a slight frequency mismatch. The discrete references $C[n]$ and $S[n]$ are multiplied with the discrete measured signal $M[n]$ to produce what are commonly referred to as the “in-phase” and “quadrature” or I and Q signals

$$I[n] = M[n] \times \cos \left[\frac{2\pi f_m n}{f_s} \right] \quad (8)$$

$$I[n] = \frac{1}{2} A_m \cos(\varphi_m) + \text{dc}_m \cos \left[\frac{2\pi f_m n}{f_s} \right] + \frac{1}{2} A_m \cos \left[\frac{4\pi f_m n}{f_s} + \varphi_m \right] \quad (9)$$

$$Q[n] = M[n] \times \sin \left[\frac{2\pi f_m n}{f_s} \right] \quad (10)$$

$$Q[n] = \frac{1}{2} A_m \sin(\varphi_m) + \text{dc}_m \sin \left[\frac{2\pi f_m n}{f_s} \right] + \frac{1}{2} A_m \sin \left[\frac{4\pi f_m n}{f_s} + \varphi_m \right]. \quad (11)$$

Since multiplying by sinusoids causes frequency shifts in the spectral components, the $I[n]$ and $Q[n]$ signals will have the A_m and dc_m components shifted in the spectrum. There will be a dc component [the first terms in (9) and (11)], which is due to the amplitude and phase of the original sinusoidal signal, a component at the original modulation that has an amplitude of dc_m , and a component at twice the modulation frequency with an amplitude of one-half A_m . The measured amplitude A_m and the phase φ_m can be calculated from the dc terms of $I[n]$ and $Q[n]$. In order to obtain the dc terms, one can filter out the unwanted ac terms by convolving $I[n]$ and $Q[n]$ with a low-pass filter $h_L[n]$ to yield what are commonly referred to the real $X[n]$ and imaginary $Y[n]$ parts of the measured sinusoid

$$X[n] = h_L[n] \otimes I[n] \quad (12)$$

$$X[n] \approx \frac{1}{2} A_m \cos(\varphi_m) \quad (13)$$

$$Y[n] = h_L[n] \otimes Q[n] \quad (14)$$

$$Y[n] \approx \frac{1}{2} A_m \sin(\varphi_m). \quad (15)$$

In the cases where it is not necessary or possible to continuously measure the amplitude A_m and the phase φ_m at the sampling frequency f_s , $h_L[k]$ will be of length N_s in order to have one complete overlap with $I[n]$ and $Q[n]$. Only the values

of $X[n]$ and $Y[n]$ corresponding to the complete overlap are needed to compute the amplitude and phase. The ac components are only completely filtered out when certain conditions are met, which will be discussed later. For most low-pass filters, the ac components will be heavily attenuated. When just the dc terms are present, the amplitude can be calculated from the real and imaginary parts as

$$A_m = 2 * \sqrt{X^2 + Y^2}. \quad (16)$$

The phase can be calculated as

$$\varphi_m = \tan^{-1} \left(\frac{Y}{X} \right). \quad (17)$$

B. Digital Lock-In for Multiple Frequencies

The technique can be easily extended to the multiple-frequency-encoded sources case by multiplying the measured signal by the reference signals at each desired frequency and then computing the amplitudes and phases for those respective frequencies. In the case of N_m modulation frequencies, the analog and discrete measured signals are

$$M(t) = \text{dc}_m + \sum_{k=1}^{N_m} A_k \cos(2\pi f_k t + \varphi_k) \quad (18)$$

$$M[n] = \text{dc}_m + \sum_{k=1}^{N_m} A_k \cos \left[\frac{2\pi f_k n}{f_s} + \varphi_k \right]. \quad (19)$$

When this measured signal is multiplied by a reference signal as in (8) and (10), the resulting $I_m[n]$ and $Q_m[n]$ signals will contain not just a dc component and a component at twice the frequency of f_m but, also, frequency components corresponding to the sums and differences of all the modulation frequencies with the reference frequency

$$I_m[n] = \sum_{k=1}^{N_m} \text{dc}_m \cos \left[\frac{2\pi f_m}{f_s} \right] + \frac{A_k}{2} \times \left(\cos \left[\frac{2\pi(f_m - f_k)n}{f_s} + \varphi_k \right] + \cos \left[\frac{2\pi(f_m + f_k)n}{f_s} + \varphi_k \right] \right) \quad (20)$$

$$Q_m[n] = \sum_{k=1}^{N_m} \text{dc}_m \sin \left[\frac{2\pi f_m}{f_s} \right] + \frac{A_k}{2} \times \left(\sin \left[\frac{2\pi(f_m - f_k)n}{f_s} + \varphi_k \right] + \sin \left[\frac{2\pi(f_m + f_k)n}{f_s} + \varphi_k \right] \right). \quad (21)$$

When one of the modulation frequencies f_k equals the reference frequency f_m , it will produce a dc term due to the amplitude and phase of the component at that frequency as in (13) and (15). Typically, there are many ac frequency components that will not be completely filtered out and will distort the final computed results for A_m and φ_m , particularly if they have been shifted to low frequencies where low-pass filtering will

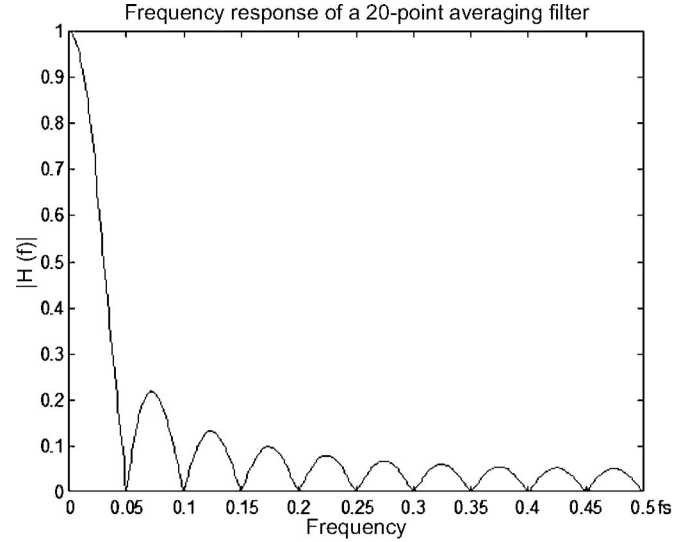


Fig. 2. Frequency response of a 20-point averaging filter.

not have a great effect. Our proposed digital lock-in detection technique is designed to be fundamentally immune to distortion from these frequency components.

III. PROPOSED DIGITAL LOCK-IN TECHNIQUE

A. Digital Low-Pass Filter and Sampling Constraints

When designing a digital lock-in filter scheme, the sampling frequency, the low-pass filter to be used, and the number of samples to be taken are all design variables. We will examine the low-pass filter first. It is well known that for the white noise, the optimum finite-impulse-response filter is a simple averaging filter that has equal coefficients at each point [18]

$$h_L[n] = \frac{1}{N_s}. \quad (22)$$

Since ac components that are not sampled for an integer number of periods contribute to the average of the finite discrete signal, the dc value computed by the averaging filter is not equal to the dc term. However, for the sampling frequency f_s , an N_s point averaging filter has a frequency response of zero at frequencies that are multiples of f_s/N_s

$$H \left(f = \frac{k f_s}{N_s} \right) = 0, \quad k \neq [0, n N_s]. \quad (23)$$

The frequency response of the filter is given by

$$H(f) = \frac{\sin \left(N_s \pi \frac{f}{f_s} \right)}{N_s \sin \left(\pi \frac{f}{f_s} \right)} e^{-j \frac{\pi (N_s - 1) f}{f_s}} \quad (24)$$

which, at low frequencies, can be approximated by

$$H(f) = \text{sinc} \left(\frac{N_s f}{f_s} \right) e^{-j \frac{\pi (N_s - 1) f}{f_s}}. \quad (25)$$

For N_s larger than ten, the bandwidth is approximately $.443 f_s / N_s$.

Fig. 2 shows the frequency response of a 20-point averaging filter. Notice that it has a response of zero at multiples of

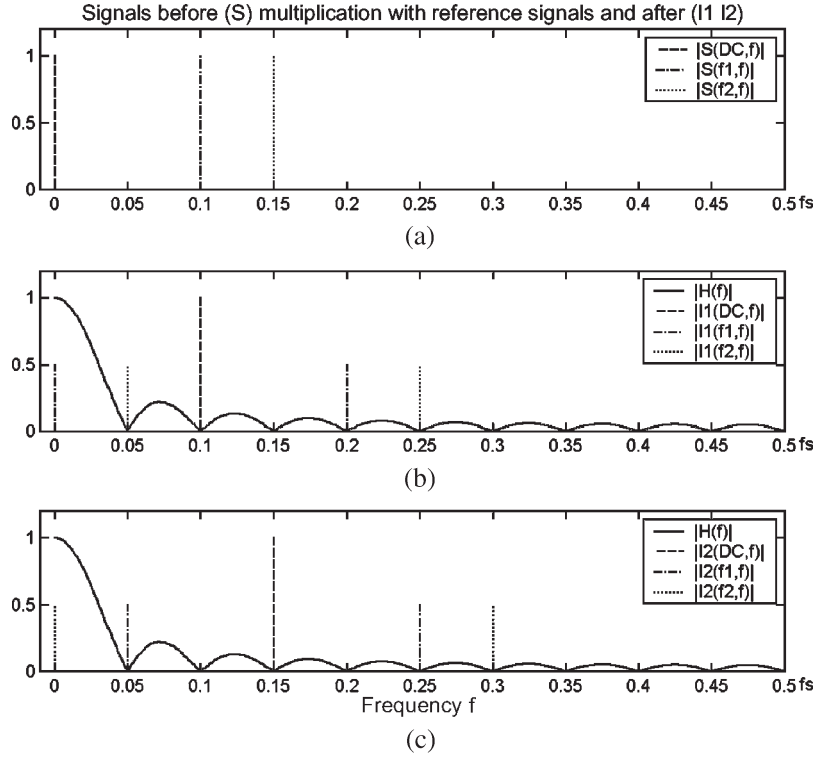


Fig. 3. Frequency-domain representation of dc, first-frequency (f_1), and second-frequency (f_2) components before and after they have been multiplied by the references to produce $I_m[n]$ signals. (a) Frequency components of the original signal. (b) Frequency components of the $I_1[n]$ signal due to multiplication with the first reference signal overlaid on the averaging-filter frequency response. (c) Frequency components of the $I_2[n]$ signal due to multiplication with the second reference signal overlaid on the averaging-filter frequency response.

$f_s/20$. This is because those frequencies are sampled for an integer number of periods. It can be made sure that the signals for each of the modulation frequencies are sampled for an integer number of periods by constraining them to the following relationship:

$$f_m = \frac{k f_s}{N_s}, \quad 1 \leq k < \frac{N_s}{2} \quad (26)$$

where k is an integer. Therefore, by careful choice of the sampling frequency f_s , the modulation frequencies f_m , and the filter length N_s , a digital lock-in scheme can have the averaging filter completely eliminate the unwanted frequency components in $X[n]$ and $Y[n]$. This is shown in Fig. 3 with the processing of two frequency components of (20). Fig. 3(b) and (c) shows the frequency components of the representative $I_1[n]$ and $I_2[n]$ signals. Notice that, for both signals, the frequencies to which the unwanted components have been shifted are also frequencies at which the filter's frequency response is zero. This means that the $X[n]$ and $Y[n]$ signals will be free from these distortions.

B. Implementation Issues

In cases where there is a need for f_m to be larger than the possible values for f_s , a heterodyne lock-in detection can be performed instead of a homodyne one. Now, the intermediate frequency (f_{IF}), which is the difference between the modulation frequency and the frequency of the local oscillator (f_{LO}), is the frequency of interest and for which the reference

sinusoid signals are needed. The intermediate frequency must be constrained by

$$f_{IF} = f_m - f_{LO} = \frac{k f_s}{N_s}, \quad 1 \leq k \leq N_s - 1. \quad (27)$$

In most cases, the ADC, which performs the sampling, is triggered by a digital controller such as the complex programmable logic device, the FPGA, or an other component. These digital controllers allow a tight timing control, which makes it fairly easy to sample at a particular sampling frequency. The digital controller operates at a clock frequency f_{clk} . The digital controller can be programmed to trigger sampling every N_c clock cycles, so that the sampling frequency is then given by

$$f_s = \frac{f_{clk}}{N_c}. \quad (28)$$

This means that, for a given clock frequency, it is not possible to realize any arbitrary sampling frequency. Digital clock oscillators are available in a wide range of frequencies, enabling another degree of freedom in realizing a desired sampling frequency. This means that one must implement modulation frequencies according to

$$f_m = \frac{k f_{clk}}{N_s N_c}, \quad 1 \leq k < \frac{N_s}{2}. \quad (29)$$

This is fairly easily accomplished with direct digital synthesis (DDS) chips, which are now widely available. Moreover, if one uses the same digital clock for the digital controller that controls both the ADC and the DDS and numerically generates

TABLE I
RESULTS OF DIGITAL LOCK-IN ALGORITHM VALIDATION

Signal	# Sources	SNR	Source Amp.	Source Phase	Calc. Amp	Calc. Phase
Num. 1	1	2	1	45°	0.992	50.7°
Num. 2	1	2	1	60°	0.996	62.5°
Num. 1 + Num. 2 (N1)	2	2	1	45°	0.992	50.7°
Num. 1 + Num. 2 (N2)	2	2	1	60°	0.996	62.5°
Exp. 1	1	11.04	unknown	unknown	1.0016	281°
Exp. 2	1	7.85	unknown	unknown	1.0005	285.7°
Exp. 1 + Exp. 2 (1)	2	6.48	unknown	unknown	1.005	280.4°
Exp. 1 + Exp. 2 (2)	2	6.48	unknown	unknown	0.997	285.5°

and stores the reference signals in the memory, there will be no frequency drift between the reference and modulation frequencies because the same clock will be responsible for the progression of phase for both the source and reference signals.

C. Computation Issues

Because applications often require real-time measurements from numerous channels in addition to multiple modulation frequencies, the computation time for the digital lock-in becomes a serious issue if the digital lock-in scheme is not efficiently implemented. It might at first appear that the whole process of multiplying an N_s point measurement with the N_s point reference signals and of taking the average is computationally intensive. This process, however, can be performed by a simple matrix multiplication, which can be implemented very efficiently in digital processors, as in (30) and (31), shown at the bottom of the page. Interestingly enough, the rows of the matrices correspond to the rows of the real and imaginary

parts of the discrete Fourier transform (DFT) matrix, which are needed to compute the DFT at that particular modulation frequency. For the digital processors that allow the efficient computation of the complex numbers, the rows of the DFT matrix can be directly used as in (32), shown at the bottom of the page. The amplitude and phase would then simply be twice the amplitude and phase of the complex number as in (16) and (17).

IV. RESULTS

To validate the functionality of the proposed digital lock-in algorithm, numerical and experimental tests were performed. For the experimental test, the sampling frequency was 50 kHz, and 100 samples were taken. The signals that were analyzed were the 5-kHz, the 7-kHz, and the sum of both 5- and 7-kHz signals. The results of both the numerical and experimental tests are summarized in Table I. For the numerical tests, the amplitude and phase were known. The digital lock-in resulted in an amplitude error of less than 0.8% and a phase error of less

$$\begin{bmatrix} X_1 \\ X_2 \\ \vdots \\ X_{N_m} \end{bmatrix} = \frac{1}{N_s} \begin{bmatrix} \cos\left(\frac{2\pi f_1 0}{f_s}\right) & \cos\left(\frac{2\pi f_1 1}{f_s}\right) & \dots & \cos\left(\frac{2\pi f_1 (N_s-1)}{f_s}\right) \\ \cos\left(\frac{2\pi f_2 0}{f_s}\right) & \cos\left(\frac{2\pi f_2 1}{f_s}\right) & \dots & \cos\left(\frac{2\pi f_2 (N_s-1)}{f_s}\right) \\ \vdots & \vdots & \ddots & \vdots \\ \cos\left(\frac{2\pi f_{N_m} 0}{f_s}\right) & \cos\left(\frac{2\pi f_{N_m} 1}{f_s}\right) & \dots & \cos\left(\frac{2\pi f_{N_m} (N_s-1)}{f_s}\right) \end{bmatrix} \times \begin{bmatrix} M[1] \\ M[2] \\ \vdots \\ M[N_s] \end{bmatrix} \quad (30)$$

$$\begin{bmatrix} Y_1 \\ Y_2 \\ \vdots \\ Y_{N_m} \end{bmatrix} = \frac{1}{N_s} \begin{bmatrix} \sin\left(\frac{2\pi f_1 0}{f_s}\right) & \sin\left(\frac{2\pi f_1 1}{f_s}\right) & \dots & \sin\left(\frac{2\pi f_1 (N_s-1)}{f_s}\right) \\ \sin\left(\frac{2\pi f_2 0}{f_s}\right) & \sin\left(\frac{2\pi f_2 1}{f_s}\right) & \ddots & \sin\left(\frac{2\pi f_2 (N_s-1)}{f_s}\right) \\ \vdots & \vdots & \ddots & \vdots \\ \sin\left(\frac{2\pi f_{N_m} 0}{f_s}\right) & \sin\left(\frac{2\pi f_{N_m} 1}{f_s}\right) & \dots & \sin\left(\frac{2\pi f_{N_m} (N_s-1)}{f_s}\right) \end{bmatrix} \times \begin{bmatrix} M[1] \\ M[2] \\ \vdots \\ M[N_s] \end{bmatrix} \quad (31)$$

$$\begin{bmatrix} X_1 - jY_1 \\ X_2 - jY_2 \\ \vdots \\ X_3 - jY_{N_m} \end{bmatrix} = \frac{1}{N_s} \begin{bmatrix} e^{\left(\frac{-j2\pi f_1 0}{f_s}\right)} & e^{\left(\frac{-j2\pi f_1 1}{f_s}\right)} & \dots & e^{\left(\frac{-j2\pi f_1 (N_s-1)}{f_s}\right)} \\ e^{\left(\frac{-j2\pi f_2 0}{f_s}\right)} & e^{\left(\frac{-j2\pi f_2 1}{f_s}\right)} & \dots & e^{\left(\frac{-j2\pi f_2 (N_s-1)}{f_s}\right)} \\ \vdots & \vdots & \ddots & \vdots \\ e^{\left(\frac{-j2\pi f_{N_m} 0}{f_s}\right)} & e^{\left(\frac{-j2\pi f_{N_m} 1}{f_s}\right)} & \dots & e^{\left(\frac{-j2\pi f_{N_m} (N_s-1)}{f_s}\right)} \end{bmatrix} \times \begin{bmatrix} M[1] \\ M[2] \\ \vdots \\ M[N_s] \end{bmatrix} \quad (32)$$

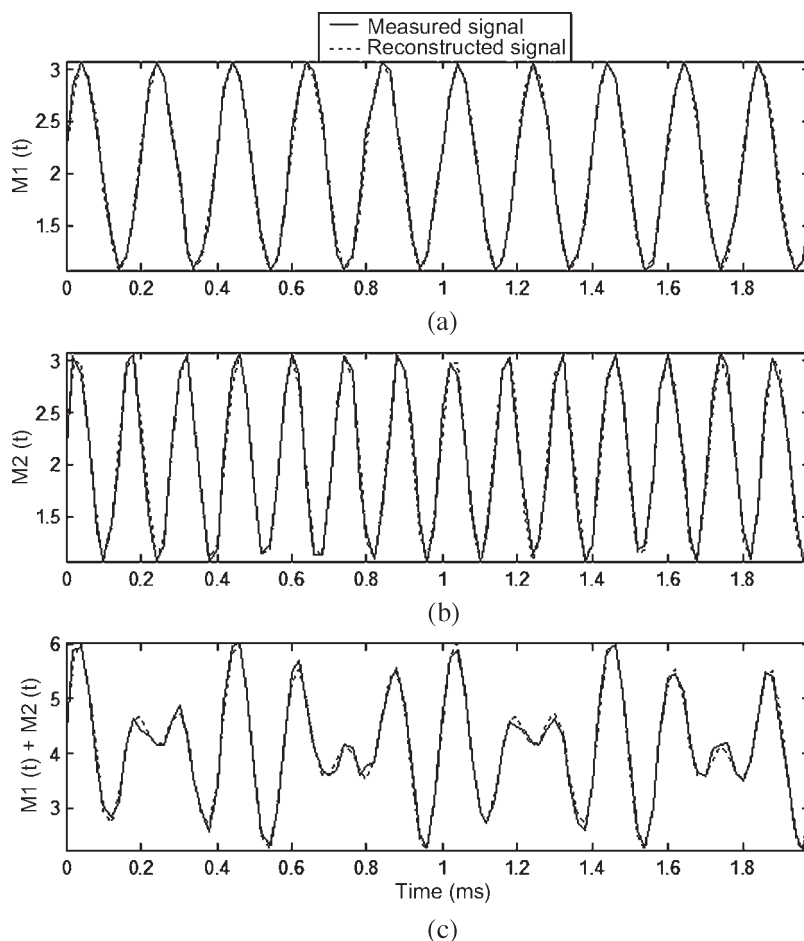


Fig. 4. Measured signals and the signals that are synthesized from calculated amplitude and phase. (a) Measured 5-kHz signal with the signal reconstructed from its calculated amplitude and phase. (b) Measured 7-kHz signal with the signal reconstructed from its calculated amplitude and phase. (c) Measured signal consisting of both 5- and 7-kHz signals along with the signal reconstructed from their respective calculated amplitudes and phases.

than 5.7° . Furthermore, the results are the same for the single- and two-frequency cases.

To experimentally test the algorithm, two light-emitting diodes were amplitude-modulated at frequencies of 5 and 7 kHz to produce unknown amplitudes that were observed to be close to one. The signal was measured by a photodetector with a transimpedance amplifier, and the signal was sampled by an oscilloscope and saved into the memory. The digital lock-in algorithm was implemented using MATLAB on a PC with an AMD Athlon XP processor. Fig. 4 shows the measured signals and the signals that are reconstructed from the calculated amplitude and phase. The first signal is the 5-kHz signal, the second one is the 7-kHz signal, and the third one is the sum of the two signals. Since the amplitude and phase are unknown until they are measured by the lock-in algorithm, one can only comment on the fact that the results change by less than 0.35% for the amplitude and less than 0.6° for the phase when the two single-frequency cases are added to produce the two-frequency case. When adding the two signals, their respective noises are added, resulting in a decrease in the signal-to-noise ratio (SNR). Moreover, the algorithm was tested in both the conventional multiply-and-take-the-mean and matrix multiplication forms in (30) and (31). The matrix multiplication method performed 200 times faster than the conventional method, even though both yielded the exact same amplitude and phase results.

Another set of numerical tests were conducted to study the performance improvement that the sampling constraints bring while using different numbers of modulation frequencies. The effect of noise was also studied by adding noise to create different SNR levels. We simulated with no noise added to produce an SNR of infinity and added noise to produce an SNR of two. For these experiments, the sampling frequency was set to 75 kHz, 150 samples were taken, and two different sets of modulation frequencies were used. The first set, which did not follow our sampling constraints, consists of 5.06, 6.13, 7.19, and 8.3 kHz. The second set consisted of 5, 6, 7, and 8 kHz, all of which followed our sampling constraints because they were multiples of 500 Hz. For each case, the digital lock-in algorithm was tested using a constant amplitude for each frequency component, random phase, and random noise. The number of modulation frequencies was varied by using either the first, the first two, the first three, or all the four modulation frequencies. The average amplitude error was calculated after running the algorithm 10 000 times for each case. Table II summarizes the results. It is apparent that when no noise is applied, there is virtually no error when following the sampling constraints. When the modulation frequencies that do not follow the sampling constraints are used, the error increases with the number of modulation frequencies employed. When noise is applied, it is clear that following the sampling constraints yields

TABLE II
RESULTS FOR DIGITAL LOCK-IN WITH DIFFERENT FREQUENCIES

SNR	# frequencies	Amplitude Error @			
		5.06 kHz	6.13 kHz	7.19 kHz	8.3 kHz
Inf	1	0.7%			
Inf	2	4.1%	4.1%		
Inf	3	4.9%	5.0%	4.5%	
Inf	4	5.7%	6.2%	7.1%	7.2%
2	1	4.7%			
2	2	6.0%	6.0%		
2	3	6.7%	6.8%	6.5%	
2	4	7.4%	7.8%	8.4%	8.5%
		5 kHz	6 kHz	7 kHz	8 kHz
Inf	1	>10 ⁻¹³ %			
Inf	2	>10 ⁻¹³ %	>10 ⁻¹³ %		
Inf	3	>10 ⁻¹³ %	>10 ⁻¹³ %	>10 ⁻¹³ %	
Inf	4	>10 ⁻¹³ %	>10 ⁻¹³ %	>10 ⁻¹³ %	>10 ⁻¹³ %
2	1	4.6%			
2	2	4.6%	4.6%		
2	3	4.5%	4.6%	4.6%	
2	4	4.6%	4.6%	4.6%	4.6%

the same performance, regardless of the number of modulation frequencies used. Using multiple modulation frequencies still adds distortion when the noise is applied. It is also evident that not following the constraints can produce errors that are very high in magnitude, depending on the sampling and modulation frequencies and the number of samples taken. Employing the modulation frequencies that do not adhere to the sampling constraints can produce results similar to adding a lot of noise to a signal. For example, when the incorrect modulation frequencies are simulated with no noise, they yield similar results with the one using the acceptable modulation frequencies and an SNR of only two.

V. CONCLUSION

We presented the digital lock-in amplification detection scheme that is ideal for applications that use multiple modulation frequencies, such as in optical and electrical impedance spectroscopy and tomography applications. The digital lock-in detection scheme utilizes sampling and modulation constraints and the unique frequency response of the averaging filter to provide optimum white-noise cancellation and source discrimination. It was shown that the amplitude and phase can efficiently be computed by performing simple matrix multiplication. Results from numerical and experimental tests show the technique's immunity to intersource distortion and its computational efficiency. Although the technique was primarily explained for homodyne detection, it could easily be extended to heterodyne detection by moving the constraints on the modulation frequencies to the heterodyne intermediate frequencies.

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